A. General Description —

The HT–12A/B are CMOS LSI designed for the digital code transmission with 38KHz carrier transmitter. The HT–12A/B encode 12 bits of information and serially transmit this information with 38KHz carrier upon receipt of a data trigger. The decoder (HT–12D) receive and decode the serial signal. When the received address matching that of the decoder's, the valid transmission (VT) output goes high and 4 bits data are latched to the output pins.

B. Features —

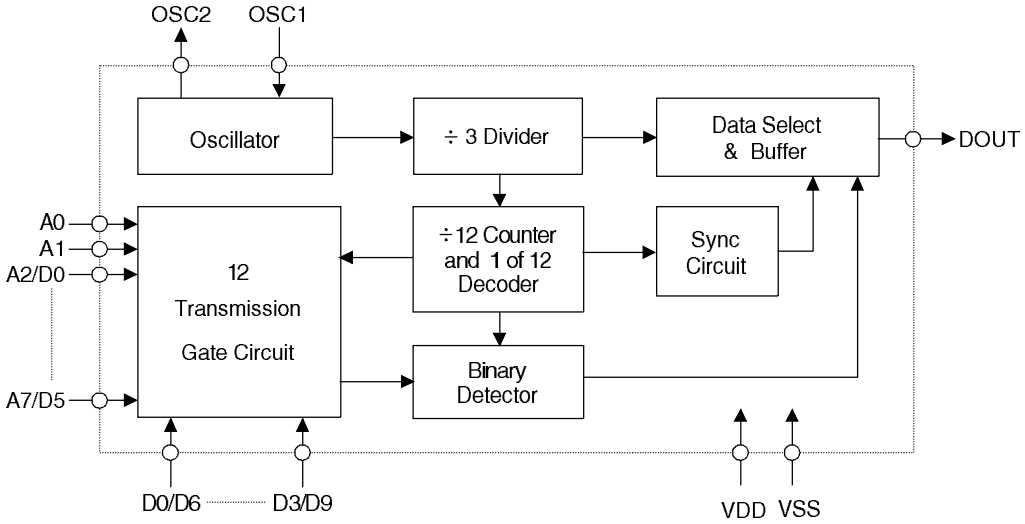
- Low power, High noise immuity CMOS technology.
- Low stand-by current: 1 μA typically.
- Wide operating voltage:
  * HT–12A, HT–12B: 2.4V ~ 5V
  * HT–12D: 2.4V ~ 12V
- 2^8 address code, 4 data output.
- Data Latch/Momentary output option.
- Easy interface with Infra-Red transmission media.
- Minimum external components.
- 18 pin plastic dual-in-line package.

C. Applications —

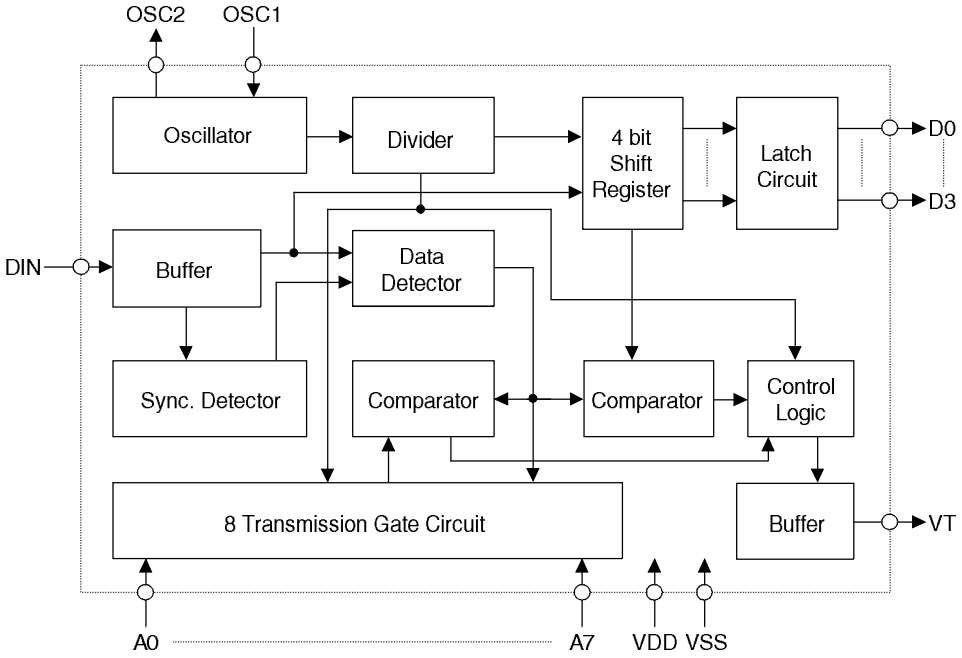
- Burglar alarm system.
- Smoke and fire alarm system.
- Garage door controller.
- Car door controller.
- Car alarm system.
- Security system.
- Cordless telephone.
- Other remote control system.

D. Block Diagram —

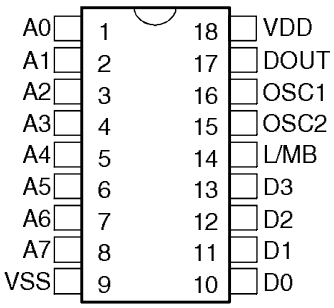
(HT–12A/B)



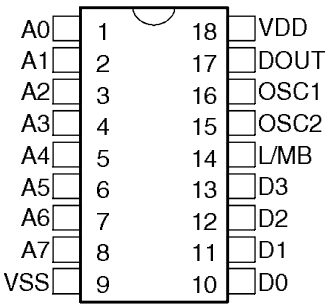
(HT–12D)



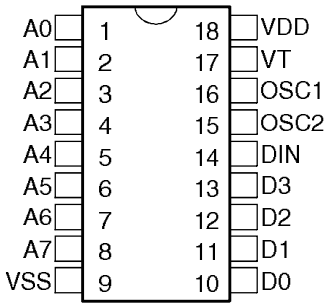
E. Pin Assignment —



HT – 12A



HT – 12B



HT – 12D

F. Pin Description —

(HT–12A/B)

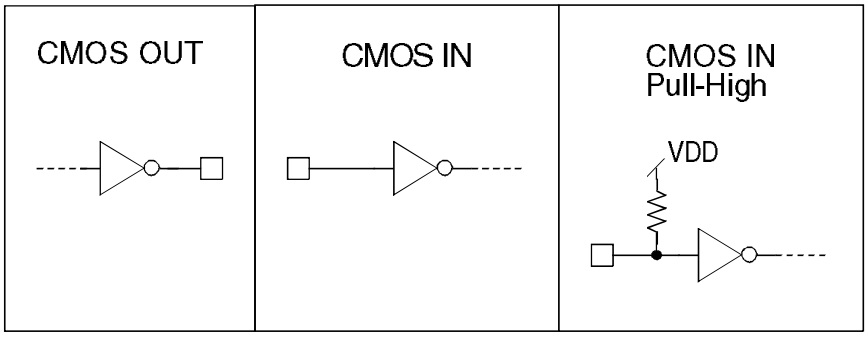
Pin No.	Pin Name	I/O	Intemal connection	Description
1~8	A0~A7	I	CMOS IN Pull High	Input pin for address A0~A7 setting.
9	VSS	I	—	Negative power supply (GND).
10~13	D0~D3	I	CMOS IN Pull High	Input pin for data D0~D3 setting, DOUT will be activated when any one of D0~D3 set to low.

Pin No.	Pin Name	I/O	Intemal connection	Description
14	L/MB	I	CMOS IN Pull High	Data Latch/Momentary Selected, Floating(or VDD) : Latch VSS : Momentary
15	OSC2	O	CMOS OUT	Oscillator output pin.
16	OSC1	I	CMOS IN	Oscillator input pin.
17	DOUT	O	CMOS OUT	Encoded data output pin.
18	VDD	I	—	Positive power supply.

(HT–12D)

Pin No.	Pin Name	I/O	Intemal connection	Description
1~8	A0~A7	I	CMOS IN Pull High	Input pin for address A0~A7 setting.
9	VSS	I	—	Negative power supply (GND).
10~13	D0~D3	O	CMOS OUT	Data output pin.
14	DIN	I	CMOS IN	Data input pin.
15	OSC2	O	CMOS OUT	Oscillator output pin.
16	OSC1	I	CMOS IN	Oscillator input pin.
17	VT	O	CMOS OUT	Valid Transmission indicator output, active high.
18	VDD	I	—	Positive power supply.

Sketchy circuit of internal connection



G. Absolute Maximum Ratings —

(Ta=25°C)

Parameter	Symbol		Minimum	Maximum	Unit
Supply Voltage	V_{DD}	HT–12A,B	–0.3	6	V
		HT–12D		13	
Input/Output Voltage	V_I		V_{SS}–0.3	V_{DD}+0.3	V
Storage Temperature	T_{STG}		–50	125	°C
Operating Temperature	T_{OP}		0	70	°C

H. Electrical Characteristics —

(HT–12A/B)

(Ta=25°C)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
		VDD	Condition				
V_{DD}	Supply Voltage	—	—	2.4	3	5	V
I_{STB}	Stand-by Current	3V	Oscillator stop	—	0.1	1	μA
		5V		—	0.1	1	
I_{DD}	Operating Current	3V	F_{OSC}=455KHz No load	—	200	400	μA
		5V		—	400	800	
Rup	Pull-up Resistance (D0~D3)	3V	V(D0~D3)=0V	—	250	500	KΩ
		5V			150	300	
I_O	Output Drive Current	5V	V_{OH}=0.9V_{DD} (Source)	–1	–1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	2	3.2	—	

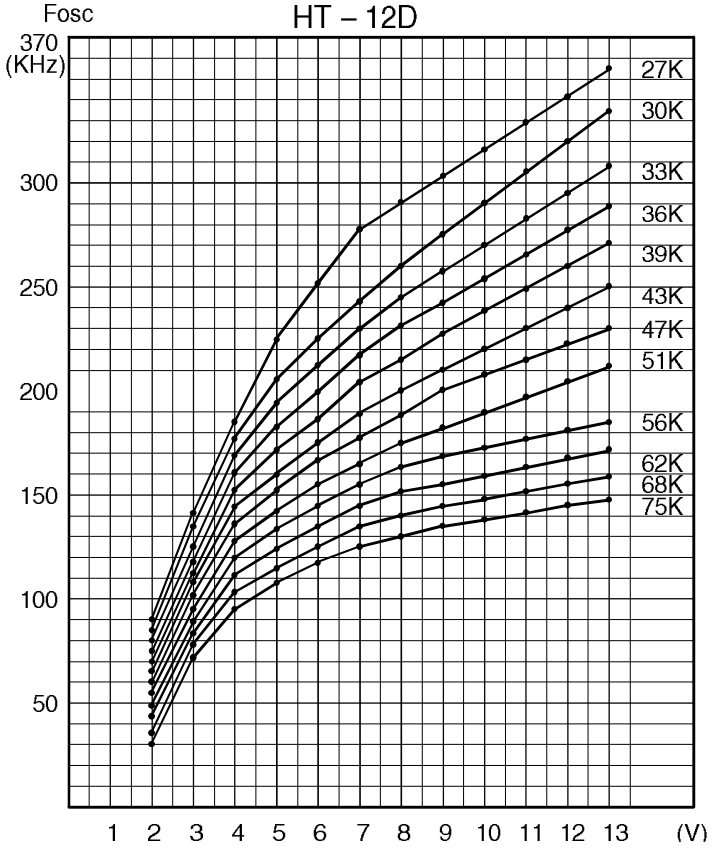
(HT–12D) (Ta=25°C)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
		VDD	Condition				
V_{DD}	Supply Voltage	—	—	2.4	—	12	V
I_{STB}	Stand-by Current	3V	cillator stop	—	0.1	1	μA
		12V		—	0.1	1	
I_{DD}	Operating Current	5V	F_{OSC}=200KHz No load	—	200	400	μA
		12V		—	600	1200	
I_{DATA}	Data Output Drive Current (D0~D3)	5V	V_{OH}=0.9V_{DD} (Source)	–1	–1.6	—	mA
			V_{OL}=0.1V_{DD} (Sink)	1.5	2.6	—	

I. Recommended Oscillator Parameters —

HT–12D	
R	F_{OSC}
75KΩ	100KHz

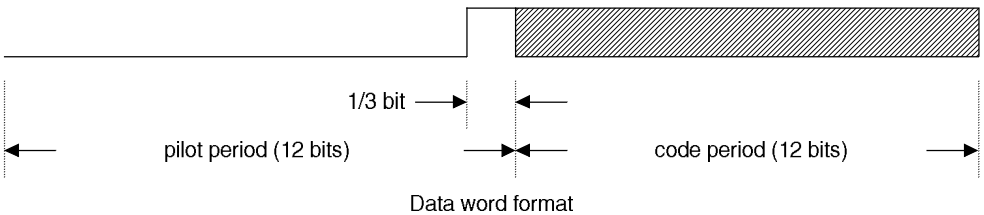
Fosc—V Curve with Rosc 75k ~ 27K



J. Function Description —

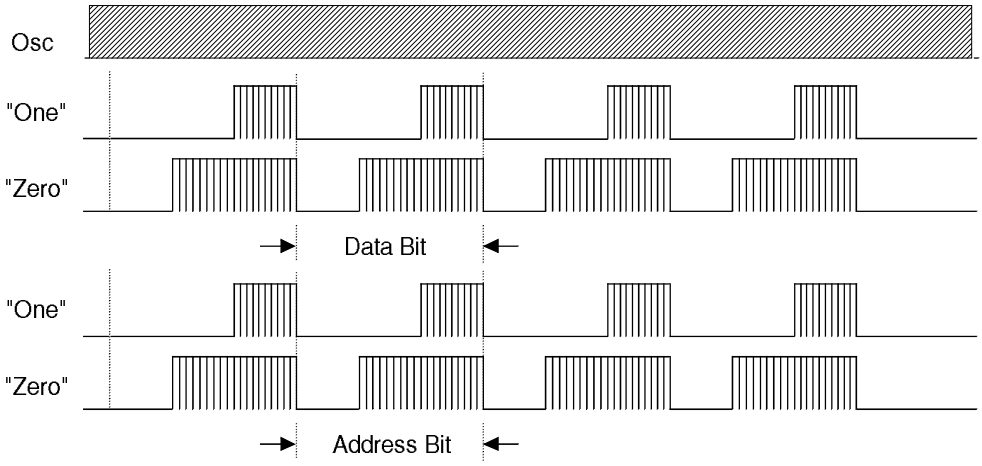
1. Encoder Operation

Upon receipt of a DATA trigger (any one of D0~D3 set to low), the HT–12A/B begins a 4 word transmission cycle and repeats this transmission cycle until the DATA trigger has been removed. One transmission cycle is composed of 4 data words each contains 2 periods: pilot and code period as shown below:

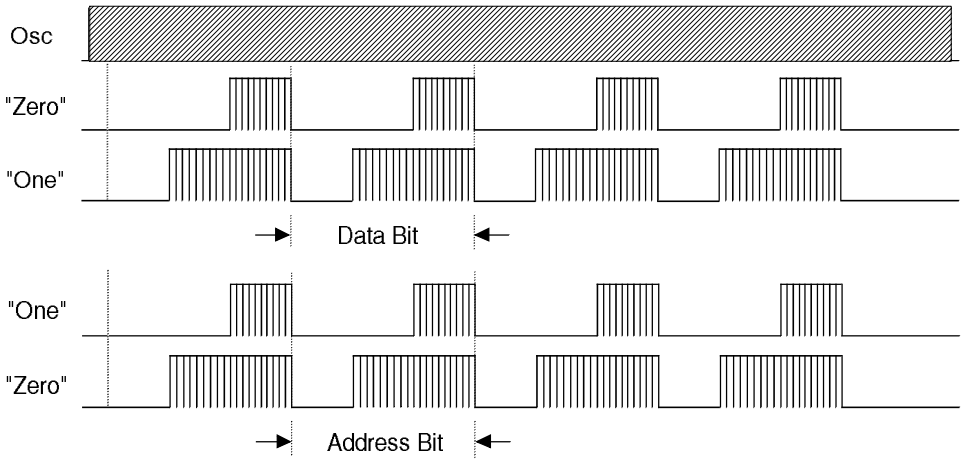


Data word format

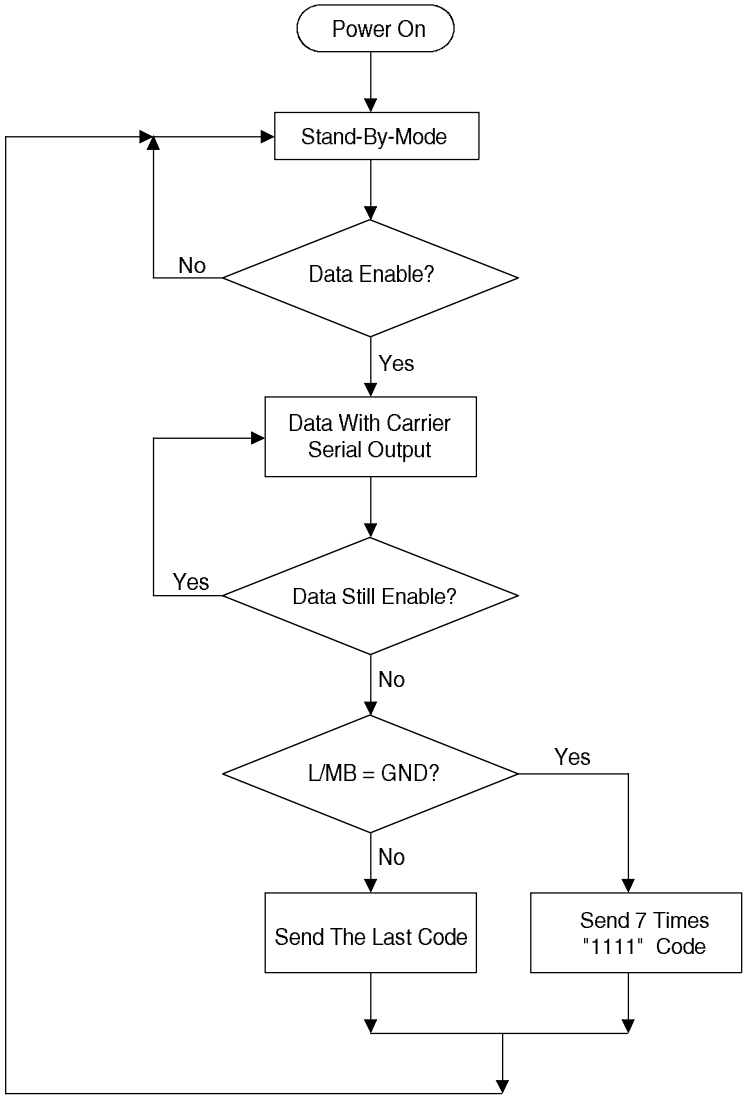
The HT–12A detects the logic state of address/data (A0~A7, D0~D3) and transmits this information during code period. Each address/data pin can be set as one of two following logic state:



The HT–12B data code polarity is inverse:



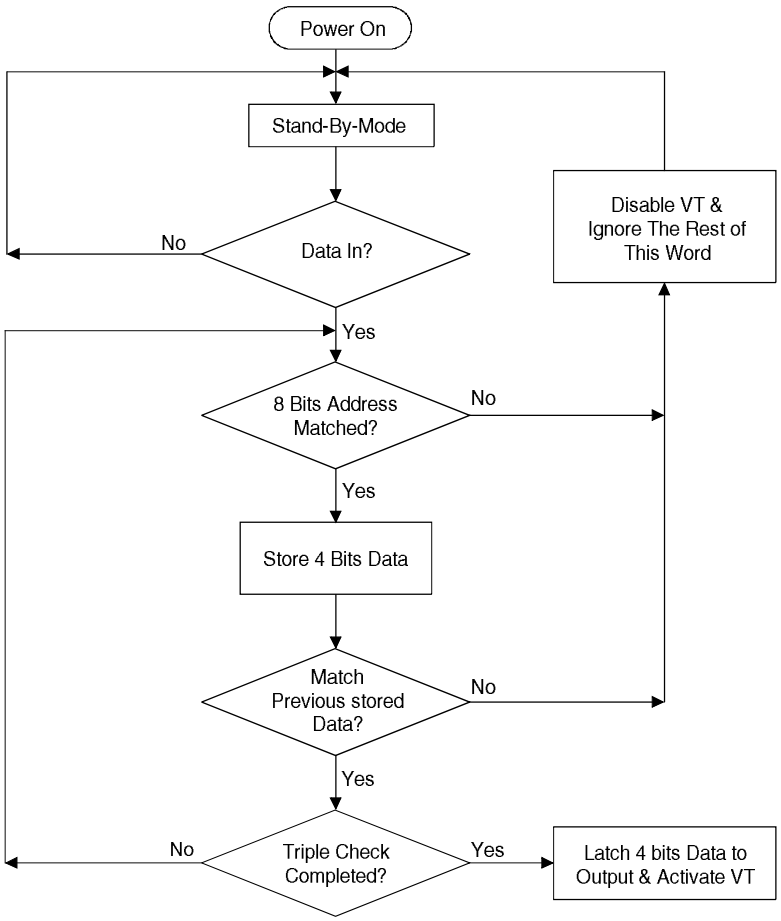
Encoder Flowchart



2. Decoder Operation

HT–12D receives the data that transmitted by HT–12A/B and interprets the first 8 bits of code perriod as address and the last 4 bits as data. The HT–12D checks the received address/data three times, if all the received address match the contents of the decoder's, 4 bits of data is decoded to activate output pins and the VT pin goes high.

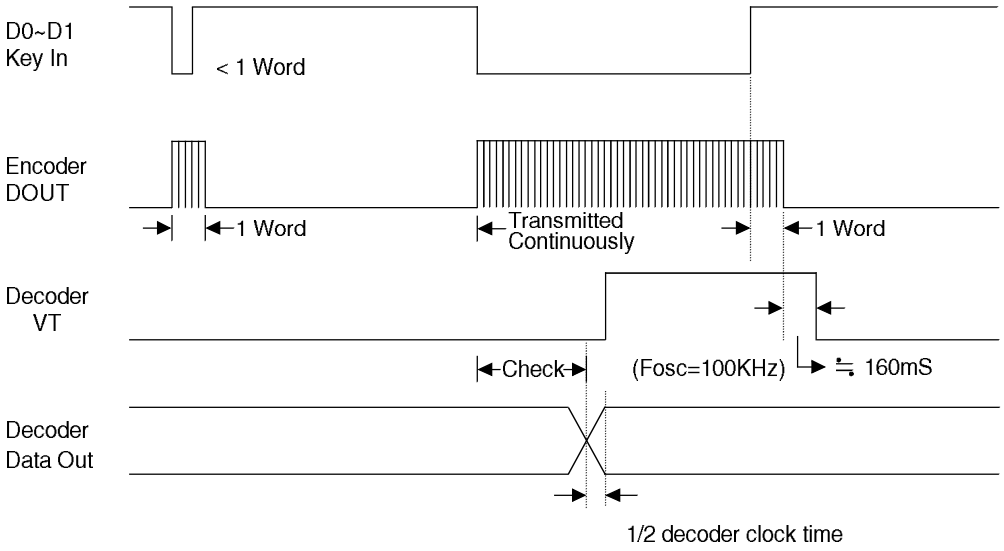
Decoder Flowchart



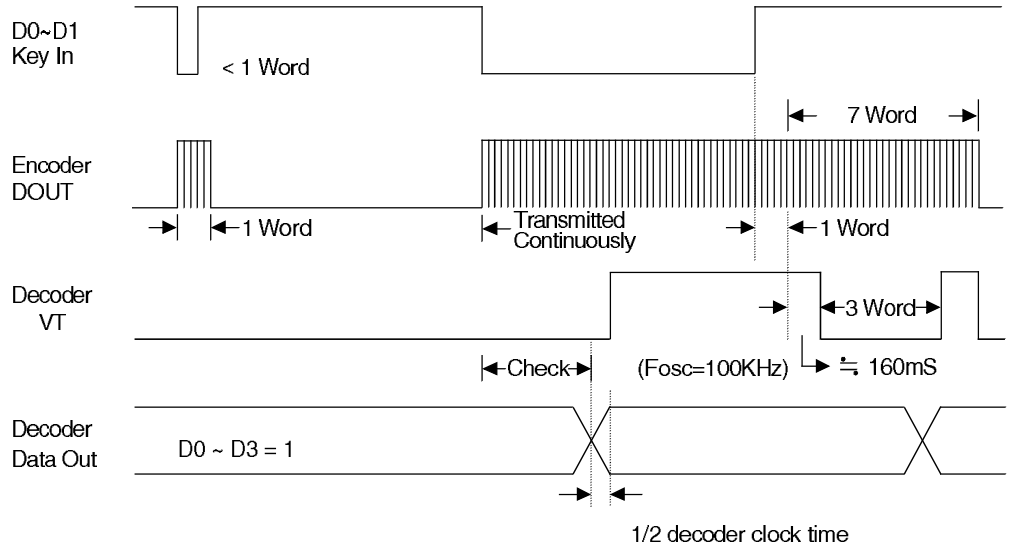
Note : The oscillator is disabled in stand-by state and activated as long as a logic "high" signal applied to DIN pin. i. e. the DIN shouled be kept in logic "low" during no signal input.

3. Encoder/Decoder Timing Diagram:

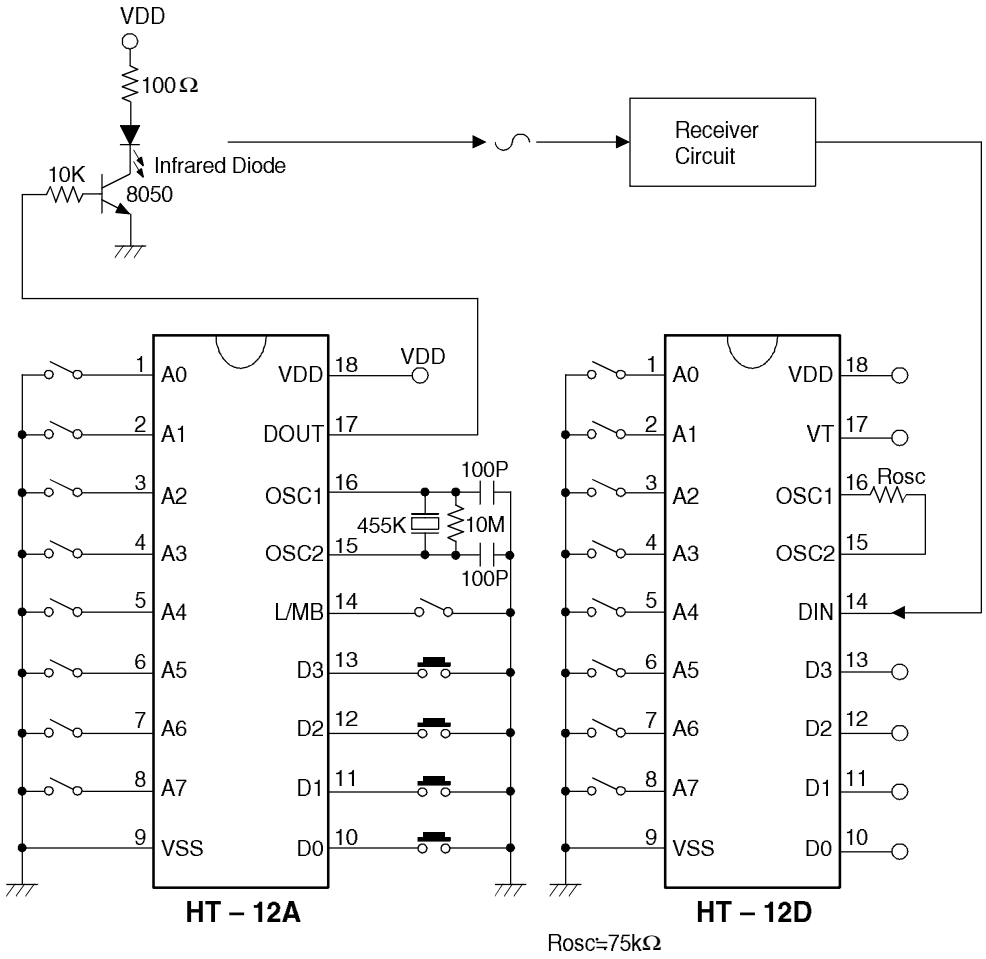
3.1: L/MB=Floating(or VDD)

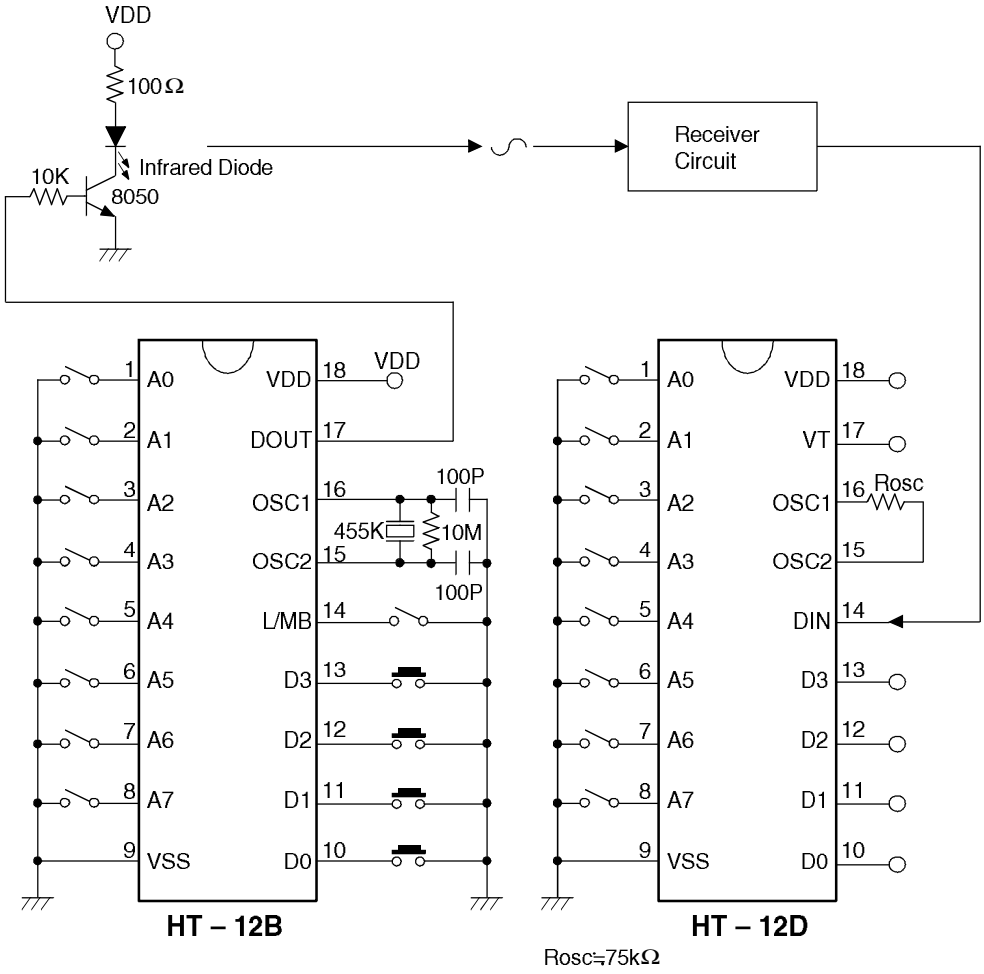


3.2: L/MB=GND



K. Application Diagram —




VDD
100Ω
Infrared Diode
10K
8050
Receiver
Circuit
A0
A1
A2
A3
A4
A5
A6
A7
VSS
VDD
DOUT
OSC1
OSC2
L/MB
D3
D2
D1
D0
100P
455K
10M
100P
HT – 12B
VT
DIN
Rosc
HT – 12D
Rosc≒75kΩ